

F10176 • F10576

HIGH SPEED HEX D FLIP-FLOP

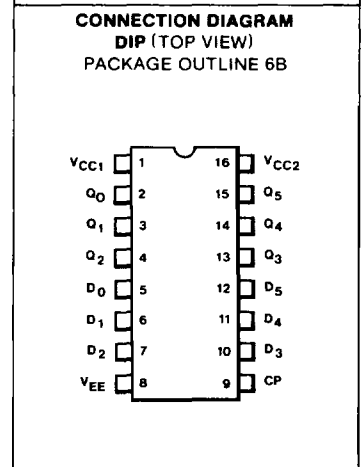
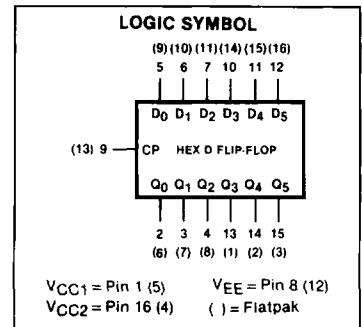
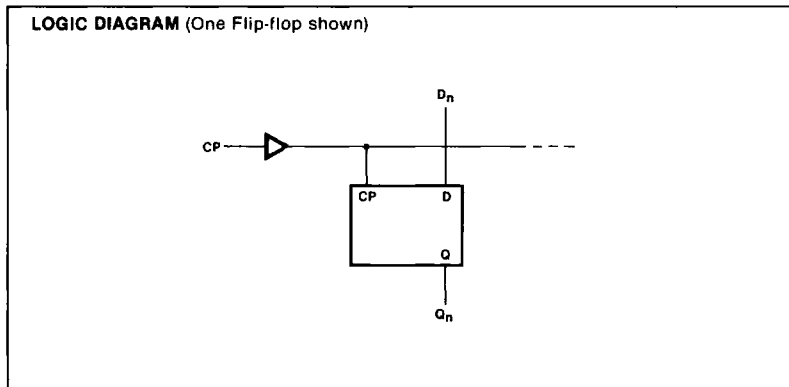
F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10176 and F10576 contain six high-speed master/slave D type flip-flops which have a common Clock. Data is entered into the master when the Clock is LOW. Data transfer takes place on the positive-going clock transition. A change in the information present at the Data input will not affect the output information.

- VOLTAGE COMPENSATED—NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS
- 50 Ω DRIVE AND WIRED-OR CAPABILITY
- SEPARATE V_{CC} PINS—ELIMINATE NOISE COUPLING
- INTERNAL 50 kΩ INPUT PULL-DOWN RESISTORS

PIN NAMES

D_n Data Inputs
 CP Clock
 Q_n Outputs



CLOCKED TRUTH TABLE

CP	D	Q _{t+1}
L	X	Q _t
H	L	L
H	H	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 t, t + 1 = Time before and after CP positive transition

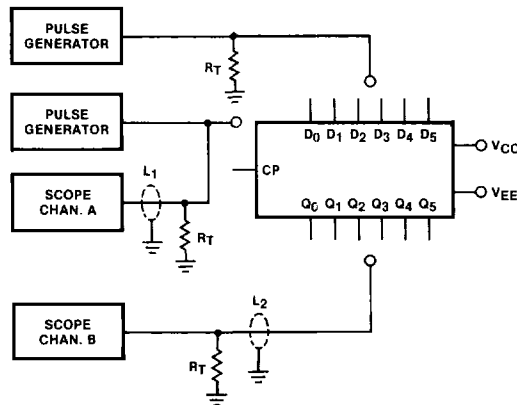
DC CHARACTERISTICS: $V_{EE} = -5.2 \text{ V}$, $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH Data Clock			220 310	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-80	-88		mA	25°C	Inputs and Outputs Open

AC CHARACTERISTICS: $V_{EE} = -5.2 \text{ V}$, $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH} , t_{PHL}	Propagation Delay LOW to HIGH, HIGH to LOW	1.5	3.0	4.5	ns	See Figure 1
t_{TLH} , t_{THL}	Transition Time, LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	
t_s	Set-Up Time	2.5			ns	
t_h	Hold Time	1.5			ns	

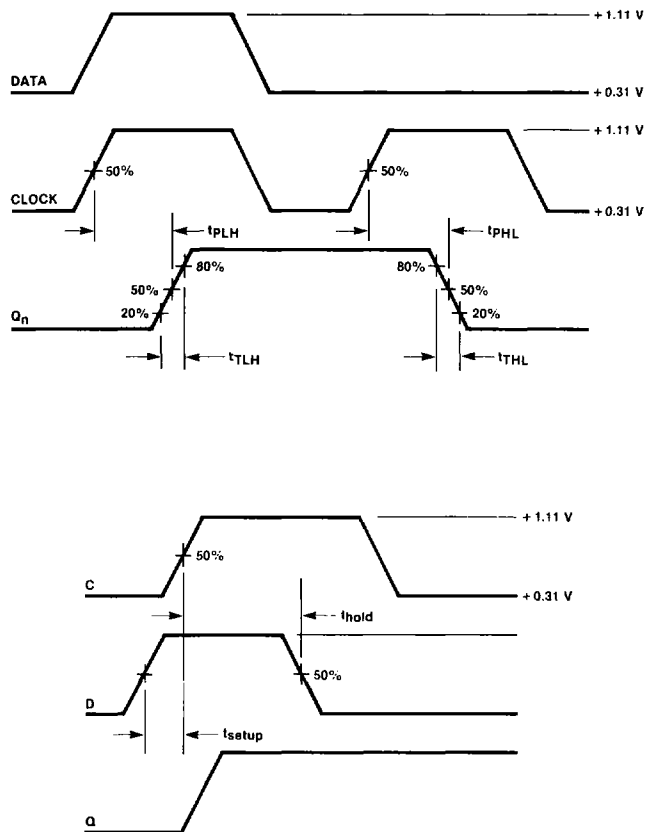
AC TEST CIRCUIT



L_1 and L_2 = equal length 50Ω impedance lines
 $R_T = 50 \Omega$ termination of scope
 $C_L = \text{Jig and stray capacitance} < 5.0 \text{ pF}$

Decoupling $0.1 \mu\text{F}$ from Gnd to V_{EE} and V_{CC}
 $V_{CC1} = V_{CC2} = 2.0 \text{ V}$
 $V_{EE} = -3.2 \text{ V}$

WAVEFORMS



t_{setup} is the minimum time before the transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D). Note that t_{hold} may be a negative number.

Figure 1